DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 45, 47-50, 54-56, 58-60 and 63 are rejected under 35 U.S.C. 102(e) as being anticipated by **Tanaka et al** (USPN 6,815,733).

Regarding claim 45, **Tanaka et al** disclose a semiconductor arrangement comprising at least one nonvolatile memory cell with a first electrode comprising at least two layers and an organic material, the organic material forming a compound with that layer of the first electrode which is in direct contact, the semiconductor arrangement produced by:

providing a first electrode comprising at least two layers (ITO/Cu) and a layer of the first electrode forms a compound (Cu-TCNQ) with an organic material [see Fig. 19];

contacting the first electrode with an organic material in order to form a compound [see col. 14, line 64 to col. 15, line 16]; and

forming a second electrode (Al) on the compound formed [see Fig. 19].

Regarding claim 47, **Tanaka et al** disclose the semiconductor arrangement of claim 45, furthermore wherein the organic material is an electron acceptor [see col. 1, lines 14-17].

Regarding claim 48, **Tanaka et al** disclose the semiconductor arrangement of claim 47, furthermore wherein the electron acceptor has electron-attracting atoms or groups, specifically –CN [i.e. since TCNQ has four –CN groups thereon].

Regarding claim 49, **Tanaka et al** disclose the semiconductor arrangement of claim 45, furthermore wherein the organic material forms a charge transfer complex with the bottom electrode [see col. 1, lines 14-17 and Fig. 19].

Regarding claim 50, **Tanaka et al** disclose the semiconductor arrangement of claim 45, furthermore wherein that layer of the first electrode which is in contact with the organic material contains copper [see Fig. 19].

Regarding claim 54, **Tanaka et al** disclose the semiconductor arrangement of claim 45, furthermore wherein the second electrode is made of aluminum [see Fig. 19].

Regarding claims 55 and 56, **Tanaka et al** disclose the semiconductor arrangement of claim 45, furthermore wherein the cell can be switched between an ON state and an OFF state, and wherein the ON and OFF states have different electrical resistances [see col. 1, lines 8-9, wherein the device disclosed by **Tanaka et al** is a switching element which functions in response to a change in applied voltage, which requires the claimed limitations].

Regarding claim 58, **Tanaka et al** disclose a method for producing a nonvolatile memory cell comprising:

providing a first electrode comprising at least two layers (ITO/Cu) and an organic material (Cu-TCNQ) [see Fig. 19];

forming a compound with the organic material and a layer of the first electrode [see col. 14, line 64 to col. 15, line 16];

contacting the electrode with an organic material in order to form a compound; and

forming a second electrode (Al) on the compound formed [see Fig. 19].

Regarding claims 59 and 63, **Tanaka et al** disclose the method of claim 58, further comprising vapor depositing the organic material onto the electrode under reduced pressure, specifically 0.0003 mbar [see col. 7, lines 37-41].

Regarding claim 60, **Tanaka et al** disclose the method of claim 58, further comprising dissolving the organic material in a solvent in the process of contacting the first electrode [see col. 14, lines 5-7].

3. Claim 82 is rejected under 35 U.S.C. 102(e) as being anticipated by **Hui** (US Patent Application Publication 2005/0227382).

Regarding claim 82, **Hui** discloses a method for producing a semiconductor arrangement comprising:

forming at least one first interconnect **408** on a substrate, which serves as a first electrode for a memory cell;

depositing an insulating layer **412**;

patterning the insulating layer, so that in insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied [see Fig. 6];

depositing an organic material **426**;

depositing at least one second electrode **428**, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell [see Fig. 9].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Nakayama** (USPN 5,943,154).

Regarding claim 46, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** do not disclose wherein the organic material has at least one of the following material of compounds: sulfur, selenium and tellurium either in pure or in bonded form in particular as organocompounds of sulfur, selenium and tellurium, and sulfur-, selenium- and tellurium-containing oligomers or polymers and one of the compounds listed in the tables of claim 45. **Nakayama** discloses an extensive list of organic compounds for use in a similar semiconductor arrangement, wherein organocompounds of sulfur are specified, namely 1,5-dimethylnaphthalene, 1,8-dimethylnaphthalene, phenothiazine, N-methylphenothiazine, naphthalene and others, and furthermore organocompounds of selenium and tellurium [see col. 10, lines 25 to col. 26, line 60]. It would have been obvious to one of ordinary skill in the art at the time of invention to use any of the compounds disclosed by **Nakayama** in the semiconductor arrangement of **Tanaka et al** because **Nakayama** teaches that these molecules are beneficially donor molecules.

6. Claims 51, 52 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733).

Regarding claim 51, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** do not disclose wherein the organic material is present in a film thickness of between 30 and 1000 nm. However, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B). In the instant case, there is no evidence to suggest that the thickness of the organic material film is critical, and furthermore it would be within the realm of reasonable experimentation for one of ordinary skill in the art to determine the film thickness that results in the desired electrical properties.

Regarding claim 52, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** do not disclose wherein the cell is scalable up to an area of 40 nm^2. However, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Regarding claim 57, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** do not disclose wherein the ratio between the ON and OFF states is more than 66. However, **Tanaka et al** teach the claimed semiconductor configuration and furthermore materials

in accordance with the instantly disclosed and claimed invention; therefore, it is reasonable to assume that the structure of **Tanaka et al** would achieve the claimed ratio between the ON and OFF states. See *In re Swinehart*, 169 USPQ 226, 229 (CCPA 1971) (where the Patent Office has reason to believe that a functional limitation asserted to be critical for establishing novelty in the claimed subject matter may, in fact, be an inherent characteristic of the prior art, it possesses the authority to require the applicant to prove that subject matter shown to be in the prior art does not possess the characteristics relied on) and *In re Fitzgerald*, 205 USPQ 594 (CCPA 1980) (the burden of proof can be shifted to the applicant to show that subject matter of the prior art does not possess the characteristic relied on whether the rejection is based on inherency under 35 USC 102 or obviousness under 35 USC 103). Note that as long as there is evidence of record establishing inherency, failure of those skilled in the art to contemporaneously recognize an inherent property, function or ingredient of a prior art reference does not preclude a finding of anticipation. See *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1349, 51 USPQ2d 1943, 1948 (Fed. Cir. 1999) (Two prior art references disclosed blasting compositions containing water-in-oil emulsions with identical ingredients to those claimed, in overlapping ranges with the claimed composition. The only element of the claims arguably not present in the prior art compositions was "sufficient aeration … entrapped to enhance sensitivity to a substantial degree." The Federal Circuit found that the emulsions described in both references would inevitably and inherently have "sufficient aeration" to sensitize the compound in the claimed ranges based on the evidence of record (including test data and expert testimony). This finding of inherency was not defeated by the fact that one of the references taught away from air entrapment or purposeful aeration.). See also *In re King*, 801 F.2d 1324, 1327, 231 USPQ 136, 139 (Fed. Cir. 1986); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 782, 227 USPQ 773, 778 (Fed. Cir. 1985).

7. Claim 53 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Idehara** (USPN 6,859,389).

Regarding claim 53, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** disclose wherein that layer of the first electrode which is not in contact with the organic material is indium tin oxide (ITO) rather than titanium (Ti), titanium nitride (TiN), tantalum (Ta), tantalum nitride (TaN), tungsten (W), TiW, TaW, WN, WCN, IrO, RuO, SrRuO or a combination of said layers and/or materials and, if appropriate, is additionally provided with a layer made of Si, TiNSi, SiON, SiO, SiC and SiCN. **Idehara** discloses a nonvolatile memory device having an electrode, wherein the electrode material may be indium tin oxide (ITO), titanium (Ti), tungsten (W) or tantalum (Ta). It would have been obvious to one of ordinary skill in the art at the time of invention to use any of the materials of **Idehara** for the electrode layer of **Tanaka et al** because **Idehara** teaches that they are known alternatives to the indium tin oxide disclosed by **Tanaka et al**. Moreover, it has been held that simple substitution of one known material for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

8. Claims 61 and 64 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Yamashita et al** (USPN 5,185,208).

Regarding claims 61 and 64, **Tanaka et al** disclose the method of claim 58. **Tanaka et al** do not disclose further comprising subjecting the organic material to a thermal treatment prior to forming the second electrode. **Yamashita et al** disclose a method of forming a Cu-TCNQ complex, as disclosed by **Tanaka et al**, wherein the contacting is performed at a temperature of

100°C prior to forming a second electrode [see col. 9, lines 22-26]. It would have been obvious to one of ordinary skill in the art at the time of invention to heat the organic material because **Yamashita et al** disclose that the complexing method disclosed thereby is effective. Moreover, it has been held that simple substitution of one known method for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

9. Claim 62 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Potember et al** (USPN 4,371,883).

Regarding claim 62, **Tanaka et al** disclose the method of claim 58. **Tanaka et al** do not disclose further comprising rinsing the excess organic material with a solvent prior to forming the second electrode. **Potember et al** disclose a method of depositing an organic material, wherein the organic material is washed with acetonitrile following deposition [see col. 7, lines 49-54]. It would have been obvious to one of ordinary skill in the art at the time of invention to rinse the organic material of **Tanaka et al** by the method of **Potember et al** because **Potember et al** disclose that rinsing beneficially removes any excess neutral acceptor molecules.

10. Claims 65, 76-78, 81 and 86-88 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Hui** (US Patent Application Publication 2005/0227382).

Regarding claim 65, **Tanaka et al** disclose the method of claim 58. **Tanaka et al** do not disclose further comprising mixing the organic material in the gas phase with a carrier gas. **Hui** discloses a method of depositing an organic material, wherein the organic material is mixed in the gas phase with a carrier gas [see paragraph 0076]. It would have been obvious to one of ordinary

skill in the art at the time of invention to deposit the organic material of **Tanaka et al** by the method of **Hui** because **Hui** discloses that vapor deposition in conjunction with a carrier gas is known for the purpose. Furthermore, it has been held that simple substitution of one known method for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

Regarding claim 76, **Tanaka et al** disclose a semiconductor arrangement having a nonvolatile memory cell with a first electrode comprising at least two layers (ITO/Cu) and an organic material (Cu-TCNQ), the organic material forming a compound with that layer of the first electrode which is in direct contact [see Fig. 19]. **Tanaka et al** do not disclose specifically wherein the nonvolatile memory cells are situated directly between bit and word lines that cross one another. **Hui** disclose a memory array comprising nonvolatile memory cells **310** wherein the nonvolatile memory cells are situated directly between bit and word lines **306**, **308** that cross one another [see Fig. 3; see also paragraph 0063]. It would have been obvious to one of ordinary skill in the art at the time of invention to include the bit and word lines of **Hui** with the semiconductor arrangement of **Tanaka et al** in order to assign a particular address to each memory cell as is well known in the art.

Regarding claim 77, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 76. Furthermore, **Tanaka et al** disclose wherein the nonvolatile memory cells are present in a plurality of layers [see Fig. 19].

Regarding claim 78, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 76. Furthermore, **Hui** discloses a method of forming a memory cell, comprising:

forming at least one interconnect **408** on a substrate **102**, which serves as first electrode;

depositing an insulating layer **412**;

patterning the insulating layer, so that in the insulating layer trenches are patterned for at least one interconnect transversely with respect to the first interconnects applied [see Fig. 6];

depositing an organic material **426**; and

depositing at least one second electrode **428**, which is arranged transversely with respect to the first interconnect applied and serves as a second electrode for the memory cell [see Fig. 9].

It would have been obvious to one of ordinary skill in the art at the time of invention to form the semiconductor arrangement of **Tanaka et al** by the method of **Hui**, in the absence of detailed instructions by **Tanaka et al**, because the method of **Hui** is disclosed as useful for forming an organic nonvolatile memory cell. Furthermore, it has been held that simple substitution of one known method for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

Regarding claim 81, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 76. Furthermore, **Hui** discloses a method of depositing an organic material between two electrodes, wherein the arrangement is produced by a Cu damascene technique [see paragraph 0065]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the damascene process of **Hui** to form the semiconductor arrangement of **Tanaka et al** because damascene processes are extremely well known in the art for forming interconnects. Furthermore, it has been held that simple substitution of one known method for another to obtain predictable results is obvious. See *KSR International Co. v. Teleflex Inc.*, 82 USPQ2d 1385 (2007).

Regarding claim 86, **Tanaka et al** disclose the semiconductor arrangement of claim 45. **Tanaka et al** do not specifically disclose wherein the arrangement is configured as a memory device containing a plurality of the nonvolatile memory cells. **Hui** discloses a memory array **300** containing a plurality of the nonvolatile memory cells **310** [see Fig. 3]. It would have been obvious to one of

ordinary skill in the art at the time of invention to configure the nonvolatile memory device of **Tanaka et al** to the configuration of **Hui** because memory arrays are well known in the art.

Regarding claims 87 and 88, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 86. Furthermore to the memory array, **Hui** discloses wherein the plurality of memory cells are arranged in one plane, specifically in the XY and in the XZ or YZ plane [see Fig. 3].

11. Claims 79 and 80 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tanaka et al** (USPN 6,815,733) in view of **Hui** (US Patent Application Publication 2005/0227382) as applied to claims 65, 76-78, 81 and 86-88 above, and further in view of **Nakayama** (USPN 5,943,154).

Regarding claim 79, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 78. Neither **Tanaka et al** nor **Hui** disclose wherein the deposition of the insulating layer is effected after the deposition of the organic material. **Nakayama** discloses a method of forming an organic material **153** between two electrodes **155**, **158**, furthermore wherein an insulating layer **157** is formed after the deposition of the organic material [see Fig. 17; see also col. 60, lines 38-44]. It would have been obvious to one of ordinary skill in the art at the time of invention to form an insulating film over the organic material, as disclosed by **Nakayama**, because it is well known in the art to provide passivation for semiconductive or conductive materials.

Regarding claim 80, the prior art of **Tanaka et al** and **Hui** disclose the semiconductor arrangement of claim 77. Furthermore, **Hui** discloses a method of forming a memory cell, comprising:

forming at least one interconnect **408** on a substrate, which serves as first electrode;

depositing an insulating layer **412**;

patterning the contact holes above the first electrode [see Fig. 6];

depositing an organic material **426** into the contact holes over the first electrode [see Fig. 8]; and

depositing at least one second electrode **428**, which serves as a second electrode for the memory cell [see Fig. 9].

Neither **Tanaka et al** nor **Hui** disclose depositing a second insulating layer and patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array. **Nakayama** discloses a method of forming an organic material **153** between two electrodes **155**, **158**, furthermore wherein an insulating layer **157** is formed after the deposition of the organic material [see Fig. 17; see also col. 60, lines 38-44]. It would have been obvious to one of ordinary skill in the art at the time of invention to form an insulating film over the organic material, as disclosed by **Nakayama**, because it is well known in the art to provide passivation for semiconductive or conductive materials. Finally, it would have been obvious to pattern the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array, in order that the second electrode might be in direct contact with the organic material.

12. Claims 83-85 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Hui** (US Patent Application Publication 2005/0227382) in view of **Nakayama** (USPN 5,943,154).

Regarding claim 83, **Hui** discloses the method of claim 82. **Hui** does not disclose wherein the deposition of the insulating layer is effected after the deposition of the organic material.

Nakayama discloses a method of forming an organic material **153** between two electrodes **155, 158**, furthermore wherein an insulating layer **157** is formed after the deposition of the organic material [see Fig. 17; see also col. 60, lines 38-44]. It would have been obvious to one of ordinary skill in the art at the time of invention to form an insulating film over the organic material, as disclosed by **Nakayama**, because it is well known in the art to provide passivation for semiconductive or conductive materials.

Regarding claim 84, **Hui** discloses a method of forming a memory cell, comprising:

forming at least one interconnect **408** on a substrate, which serves as first electrode;

depositing an insulating layer **412**;

patterning the contact holes above the first electrode [see Fig. 6];

depositing an organic material **426** into the contact holes over the first electrode [see Fig. 8]; and

depositing at least one second electrode **428**, which serves as a second electrode for the memory cell [see Fig. 9].

Hui does not disclose depositing a second insulating layer and patterning the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array. **Nakayama** discloses a method of forming an organic material **153** between two electrodes **155, 158**, furthermore wherein an insulating layer **157** is formed after the deposition of the organic material [see Fig. 17; see also col. 60, lines 38-44]. It would have been obvious to one of ordinary skill in the art at the time of invention to form an insulating film over the organic material, as disclosed by **Nakayama**, because it is well known in the art to provide passivation for semiconductive or conductive materials. Finally, it would have been obvious to

pattern the second insulating layer, so that in the insulating layer trenches are patterned for at least one second interconnect, which runs transversely with respect to the first interconnects applied and covers the contact holes in the cell array, in order that the second electrode might be in direct contact with the organic material.

Regarding claim 85, the prior art of **Hui** and **Nakayama** disclose the method of claim 84. Furthermore, as discussed above, **Nakayama** discloses depositing a protective layer **157** on the organic material after the deposition of the organic material prior to further processing.

Allowable Subject Matter

13. Claims 66-75 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. The following is a statement of reasons for the indication of allowable subject matter: regarding claims 66 and 75, the prior art of record fails to teach or make reasonably obvious wherein the compound is treated with an aftertreatment reagent.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Snow whose telephone number is (571)272-8603. The examiner can normally be reached on Monday through Friday, 8:00 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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